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EXAMINER	
BODDIE, WILLIAM	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/648,153	KOYAMA, JUN	
	Examiner	Art Unit	
	WILLIAM L. BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-14,17-27,29,47-50 and 55-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,8-14,17-22,24-27,29,47-50 and 55-59* is/are rejected.

7)☒ Claim(s) *7 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/362,881.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/7/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, March 5th, 2009, the Applicant amended claims 6 and added new claims 55-59. Currently claims 6-14, 17-27, 29 and 47-50 and 55-59 are pending.

2. Furthermore Applicant is advised that this Reissue application has been redocketed to a new Examiner.

Information Disclosure Statement

3. The information disclosure statement filed May 7th, 2002 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

4. It was unclear from the Examiner's record whether this IDS was ever forwarded to the Applicant by Examiner Chow. As such it is being resent to ensure that Applicant receives notification that the May 7th, 2002 IDS was not considered as no copy of the Foreign art was included therewith.

Allowable Subject Matter

5. The indicated allowability of claims 6, 8-14, 17-22, 24-27, 29 and 47-50 is withdrawn in view of the newly discovered reference(s) of Parks, Johary, Yazaki and Runaldue. Rejections based on the newly cited reference(s) follow.

6. Claims 7 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 18-19, 22 and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Parks (US 5,471,225).

With respect to claim 18, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a first thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5),

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

wherein said memory circuit comprises at least two inverters (52, 54, R1-2 in fig. 5), said inverters comprising at least two thin film transistors and being connected with said voltage source lines (fig. 5).

With respect to claim 19, Parks discloses, the active matrix display device of claim 18 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the digital memory circuits (clear from fig. 5).

With respect to claim 22, Parks discloses, the active matrix display device of claim 18 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claim 49, Parks discloses, the active matrix display device according to claim 18 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6, 8, 11, 47, 55-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Runaldue et al. (US 5,325,338).

With respect to claim 6, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5), wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

wherein said memory circuit comprises a pair of inverters connected to each other (fig. 5; col. 6, lines 52-61), each of said inverters comprising an N-channel TFT (fig. 5).

Parks does not expressly disclose each inverter comprising both an N-channel TFT and a P-channel TFT.

Runaldue discloses, a display memory circuit which comprises a pair of inverters connected to each other (100-103 in fig. 3), each of said inverters comprising an N-channel TFT (101 and 103 in fig. 3) and a P-channel TFT (100 and 102 in fig. 3).

Runaldue and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the memory circuit of Parks with that of Runaldue.

The motivation for doing so would have been for the well-known advantage of reduced power consumption.

With respect to claim 8, Parks and Runaldue disclose, the active matrix display device of claim 6 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the digital memory circuits (clear from fig. 5).

With respect to claim 11, Parks and Runaldue disclose, the active matrix display device of claim 6 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claim 47, Parks and Runaldue disclose, the active matrix display device according to claim 6 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

With respect to claim 55, Parks discloses, a method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel (50 in fig. 5; col. 6, lines 5-36); and

supplying a voltage to a pixel electrode (36 in fig. 5) of said pixel in accordance with the data stored in said memory circuit (col. 6, lines 2-5),

wherein said memory circuit comprises at least first and second inverters (52, 54, R1-2 in fig. 5), each of said inverters comprising an n-channel TFT (fig. 5) formed over a substrate (col. 6, lines 37-39).

Parks does not expressly disclose each inverter comprising both an N-channel TFT and a P-channel TFT.

Runaldue discloses, a display memory circuit which comprises a pair of inverters connected to each other (100-103 in fig. 3), each of said inverters comprising an N-channel TFT (101 and 103 in fig. 3) and a P-channel TFT (100 and 102 in fig. 3).

Runaldue and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the memory circuit of Parks with that of Runaldue.

The motivation for doing so would have been for the well-known advantage of reduced power consumption.

each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

With respect to claim 56, Parks and Runaldue disclose, the method according to claim 55 (see above).

Parks further discloses, wherein an output terminal of said memory circuit is connected to said pixel electrode (fig. 5).

With respect to claim 57, Parks discloses, a method of operating an active matrix display device comprising the steps of:

storing a data through a switching thin film transistor (38 in fig. 5) provided at one pixel to a memory circuit (50 in fig. 5; col. 6, lines 5-36); and

supplying one of two voltages from two voltage source lines (power and ground in fig. 5) to a pixel electrode (36 in fig. 5) of said pixel in accordance with the data stored in said memory circuit (col. 6, lines 2-5),

wherein said memory circuit comprises at least first and second inverters (52, 54, R1-2 in fig. 5), each of said inverters comprising an n-channel TFT (fig. 5) formed over a substrate (col. 6, lines 37-39).

Parks does not expressly disclose each inverter comprising both an N-channel TFT and a P-channel TFT.

Runaldue discloses, a display memory circuit which comprises a pair of inverters connected to each other (100-103 in fig. 3), each of said inverters comprising an N-channel TFT (101 and 103 in fig. 3) and a P-channel TFT (100 and 102 in fig. 3).

Runaldue and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the memory circuit of Parks with that of Runaldue.

The motivation for doing so would have been for the well-known advantage of reduced power consumption.

each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

With respect to claim 58, Parks and Runaldue disclose, the method according to claim 57 (see above).

Parks further discloses, wherein an output terminal of said memory circuit is connected to said pixel electrode (fig. 5).

With respect to claim 59, Parks and Runaldue disclose, the method according to claim 57 (see above).

Parks further discloses, wherein said display device is a liquid crystal device (title).

11. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Runaldue et al. (US 5,325,338) and further in view of Johary et al. (US 5,196,839).

With respect to claims 9 and 10, Parks and Runaldue disclose, the active matrix display device of claim 6 (see above).

Neither Parks nor Runaldue expressly disclose either a digital or time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

Johary, Parks, and Runaldue are analogous art because they are all from the same field of endeavor namely display control circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks and Runaldue under either time or digital gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

12. Claims 12, 14, 17, 20-21, 24, 26-27, 29, 48 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Johary et al. (US 5,196,839).

With respect to claim 12, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a first thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5),

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

and wherein said memory circuit comprises at least second and third thin film transistors (52 and 54 in fig. 5), one of source or drain of the second thin film transistor being connected with one of said voltage source lines (upper terminal of TFT 54 is connected to power in fig. 5), a gate electrode of the third thin film transistor (upper terminal of 54 is connected to gate of 52), and one of source or drain of the first thin film transistor (upper terminal of 54 is connected to 38 in fig. 5),

the other of source or drain of the second transistor being connected with the other of said voltage source lines (lower terminal of TFT 54 is connected to ground in fig. 5) and one of source or drain of the third thin film transistor (lower terminal of both 52 and 54 are both connected to ground), and

a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, one of said voltage source lines, and said pixel electrode (fig. 5).

Parks does not expressly disclose a time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

Johary and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks using time gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

With respect to claim 14, Parks and Johary disclose, the active matrix display device of claim 12 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the digital memory circuits (clear from fig. 5).

With respect to claim 17, Parks and Johary disclose, the active matrix display device of claim 12 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claims 20-21, Parks discloses, the active matrix display device of claim 18 (see above).

Parks does not expressly disclose either a digital or time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

Johary and Parks are analogous art because they are from the same field of endeavor namely display control circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks using time or digital gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

With respect to claim 24, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a first thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5),

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

wherein said memory circuit comprises at least two thin film transistors (52 and 54 in fig. 5), having a same conductivity type (fig. 5).

Parks does not expressly disclose a time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

Johary and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks using time gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

With respect to claim 26, Parks and Johary disclose, the active matrix display device of claim 24 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the memory circuits (fig. 5).

With respect to claim 27, Parks and Johary disclose, the active matrix display device of claim 24 (see above).

Johary further discloses, wherein the active matrix display device includes a digital gradation display device (fig. 1c).

With respect to claim 29, Parks and Johary disclose, the active matrix display device of claim 24 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claim 48, Parks and Johary disclose, the active matrix display device according to claim 12 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

With respect to claim 50, Parks and Johary disclose, the active matrix display device according to claim 24 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

13. Claims 13 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Johary et al. (US 5,196,839) and further in view of Yazaki et al. (US 4,850,676).

With respect to claims 13 and 25, Parks and Johary disclose, the active matrix display device of claims 12 and 24 (see above).

Neither Parks nor Johary expressly disclose wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average.

Yazaki discloses, wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average (col. 16, lines 3-5).

Yazaki, Parks and Johary are analogous art because they are both from the same field of endeavor namely display control circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to supply a voltage to the electro-optical modulating layer of Parks and Johary that is substantially zero on time average as taught by Yazaki.

The motivation for doing so would have been to guard against deterioration of the liquid crystal (Yazaki; col. 16, lines 5-6).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William L Boddie/
Examiner, Art Unit 2629
5/12/2010